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SERIAL NO.: 09/929,515

FILING DATE: 8/14/01

APPLICANT(S): Muthukumaraswamy, et al.

GROUP ART UNIT: 2182



**SUPPLEMENTAL  
INFORMATION DISCLOSURE CITATION  
(PTO-1449)**

**U.S. PATENT DOCUMENTS**

*		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
C	A	5,696,959	12/97	Guttag, et al.	385	595	
	B	5,696,954	12/97	Guttag, et al.	395	562	
	C	5,680,339	10/97	Moyse, et al.	364	745	
	D	5,644,790	07/97	Li, et al.	395	883	
	E	5,644,524	07/97	Van Aken, et al.	364	766	
	F	5,644,522	07/97	Moyse, et al.	364	745.02	
	G	5,625,836	04/97	Barker, et al.	395	800	
	H	5,606,677	02/97	Balmer, et al.	395	384	
	I	5,603,012	02/97	Sotheran	395	500	
	J	5,600,847	02/97	Guttag, et al.	395	800	
	K	5,590,350	12/96	Guttag, et al.	395	800	
	L	5,590,345	12/96	Barker, et al.	395	800	
	M	5,588,152	12/96	Dapp, et al.	395	800	
	N	5,577,213	11/96	Avery, et al.	395	280	
	O	5,522,082	05/96	Guttag, et al.	395	800	
	P	5,512,896	04/96	Read, et al.	341	65	
	Q	5,511,211	04/96	Akao, et al.	395	800	
	R	5,504,920	04/96	Biggs, et al.	395	800	
	S	5,479,166	12/95	Read, et al.	341	65	
	T	5,404,555	04/95	Liu	395	800	
	U	5,379,388	01/95	Asghar	395	375	
	V	4,744,054	05/88	Kawata, et al.	365	104	
	W	4,734,856	03/88	Davis	364	300	
	X						
	Y						
	Z						

CA  
Examiner

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**U.S. PATENT DOCUMENTS**

*		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
C	A	5,361,373	11/1994	Gilson	712	1	
	B	5,537,601	07/1996	Kimura, et al.	712	35	
	C	5,600,845	02/1997	Gilson	712	39	
	D	5,687,325	11/1997	Chang	712	34	
	E	5,696,956	12/1997	Razdan, et al.	712	23	
	F	5,825,202	10/1998	Tavana et al.	326	39	
	G	6,011,407	01/2000	New	326	39	
	H	6,020,755	02/2000	Andrews, et al.	326	39	
	I	5,628,028	05/97	Michelson	395	828	3/2/95
	J	5,737,631	04/98	Trimberger	395	800.37	4/5/95
	K	5,819,064	10/6/98	Razdan, et al.	395	500	11/8/95
	L	5,857,109	01/1999	Taylor	395	800	4/11/95
	M	6,028,463	02/2000	Albu, et al.	327	291	10/15/97
C	N	6,138,229	10/2000	Kucukcakar, et al.	712	37	5/29/98

**OTHER**

C 1. R.D. Witting, et al., One Chip: An FPGA Processor With Reconfigurable Logic, Proceedings of the IEEE Symposium on FPGAs for Custom Computing Machines, 1996, pp. 126-135

C 2. J.R. Hauser, et al., Garp: A MIPS Processor with a Reconfigurable Coprocessor, IEEE Symposium on FPGAs for Custom Computing Machines, 1997, pp. 12-21

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